**ECE2277A Lab 3: Multiplexers**

**Laboratory Report**

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**Boolean Function**

Please write your canonical Boolean function here as a sum of minterms (*mp*+*mq*, etc.) for reference:

*f*(*a*,*b*,*c*,*d*) = m0 + m1 + m2 + m4 + m10 + m12 + m13 + m14

The truth table for this function is:

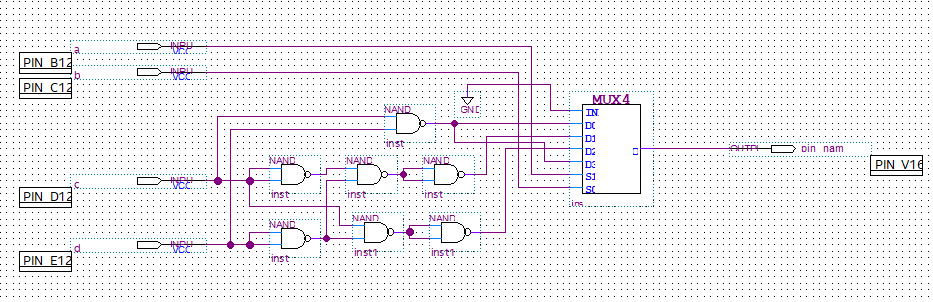
|  |  |
| --- | --- |
| *abcd* | *f*(*a*,*b*,*c*,*d*) |
| 0000 | 1 |
| 0001 | 1 |
| 0010 | 1 |
| 0011 | 0 |
| 0100 | 1 |
| 0101 | 0 |
| 0110 | 0 |
| 0111 | 0 |
| 1000 | 0 |
| 1001 | 0 |
| 1010 | 1 |
| 1011 | 0 |
| 1100 | 1 |
| 1101 | 1 |
| 1110 | 1 |
| 1111 | 0 |

**Multiplexer Enable**

The 4×1 multiplexer in Quartus is enabled by connecting INH to [*vCC*/***ground***]. This is *active* [*high*/***low***].

**Multiplexer Circuit**

Include an image of the circuit from Quartus. Add extra space if necessary.



The NAND logic function for the multiplexer inputs is:

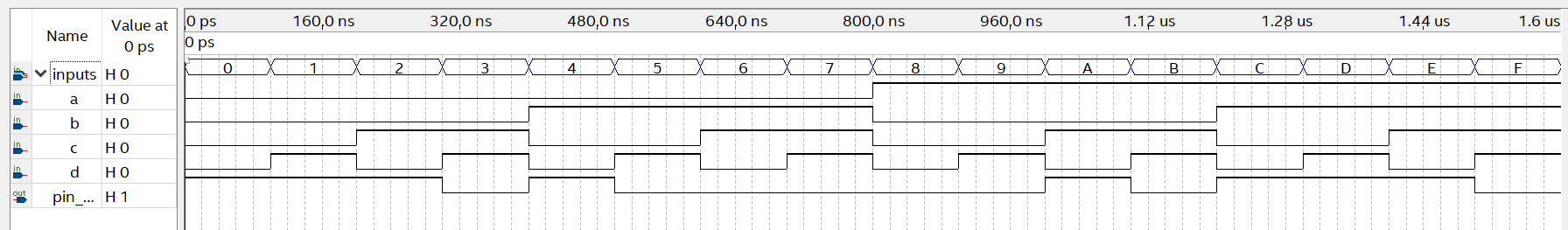
*D*0(*c*,*d*) = NAND(C,D)

*D*1(*c*,*d*) = NAND(NAND(NAND(C,C), NAND(D,D)))

*D*2(*c*,*d*) = NAND(C,D)

*D*3(*c*,*d*) = NAND(NAND(C, NAND(D,D)))

Include an image of the simulated waveforms demonstrating the correct output of the circuit. Add extra space if necessary.



**Design Questions**

Compare the present multiplexer circuit to your previous AND-OR-NOT circuits for the same Boolean function and answer the questions below. One or two sentences is sufficient. Add extra space if necessary.

1. Which circuit has the lowest cost (check the gate-based implementation of the multiplexer)?
2. Which circuit has the shortest total propagation time?
3. Finally, we designed the multiplexer circuit using *a* and *b* as control variables and *c* and *d* as data variables, but really this is an arbitrary choice. Can the cost of your multiplexer circuit be reduced if this is changed (for example, use *a*, *d* for control and *b*, *c* for data)?